FIG. 1

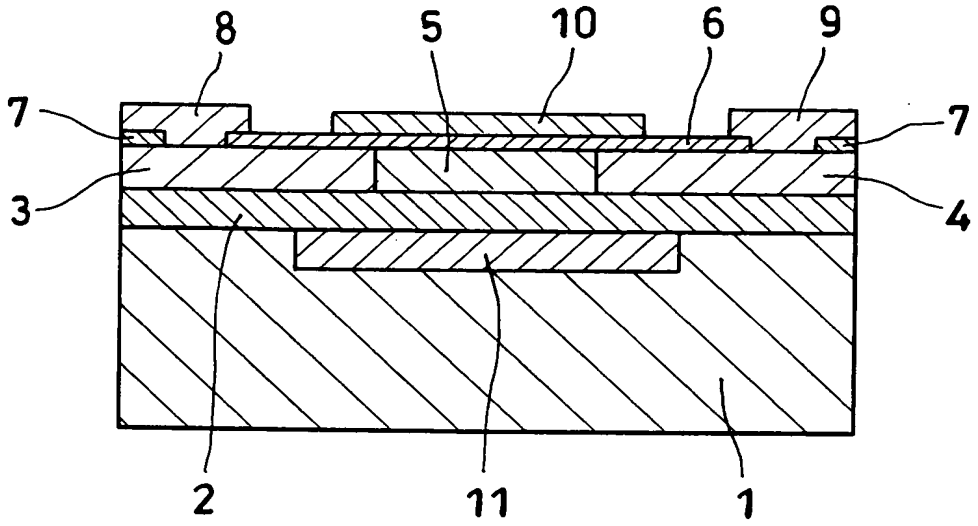

8
5
10
6
9
7
7
3
4
2
11
1

FIG. 2

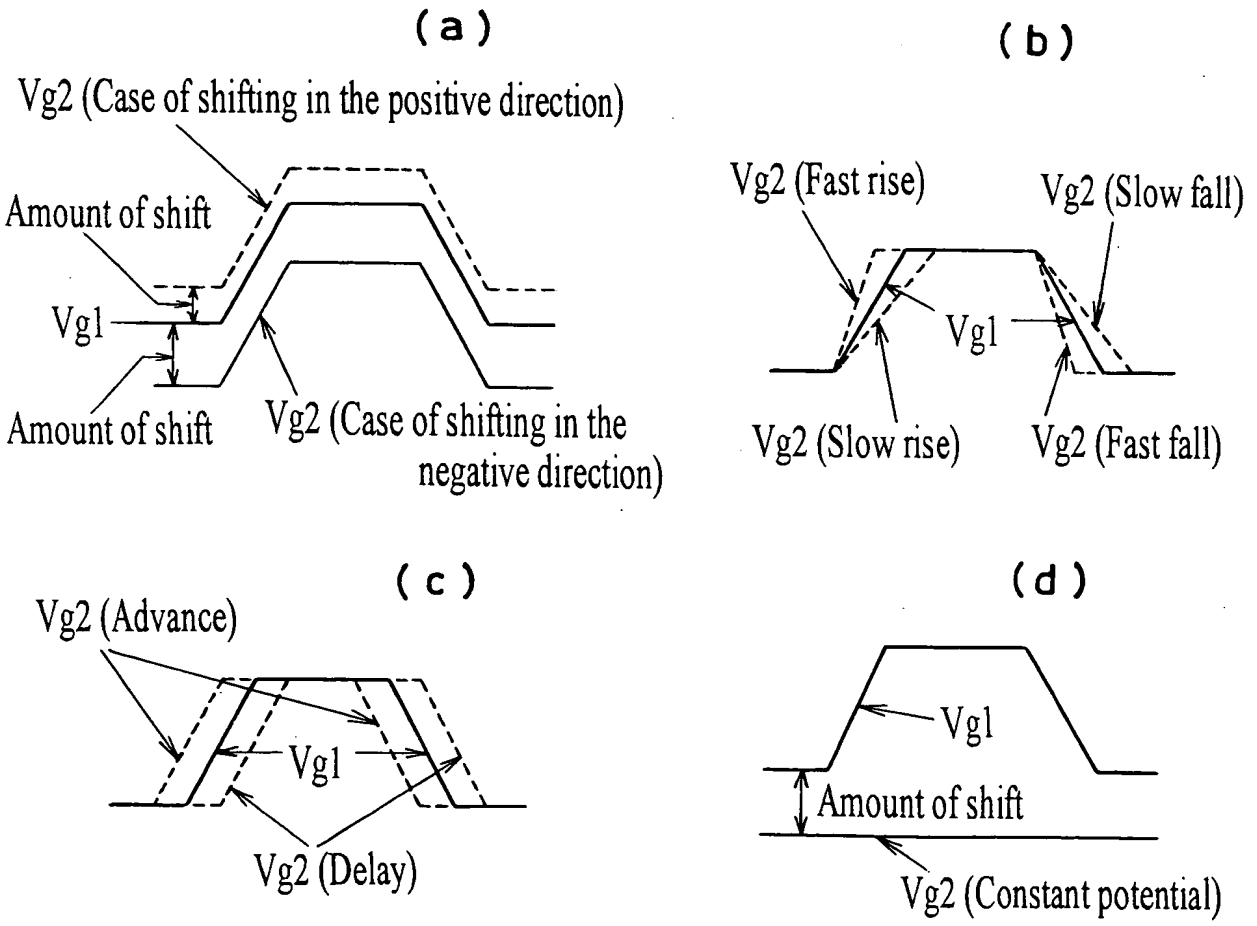

(a)
Vg2 (Case of shifting in the positive direction)
Amount of shift
Vg1
Amount of shift
Vg2 (Case of shifting in the negative direction)
(b)
Vg2 (Fast rise)
Vg2 (Slow fall)
Vg1
Vg2 (Slow rise)
Vg2 (Fast fall)
(c)
Vg2 (Advance)
Vg1
Vg2 (Delay)
(d)
Vg1
Amount of shift
Vg2 (Constant potential)

FIG. 3

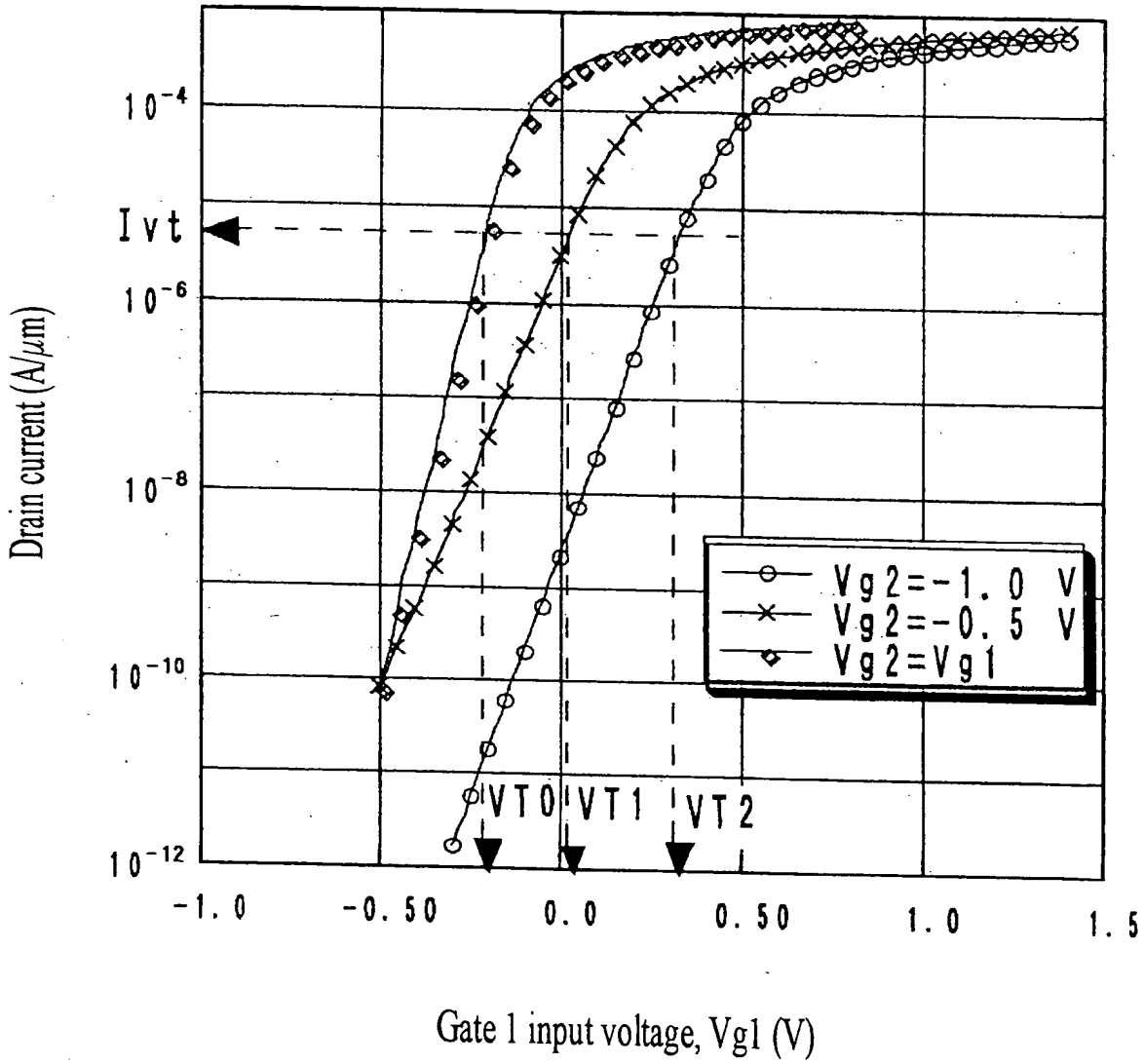

Drain current (A/μm)
10^-4
Ivt
10^-6
10^-8
10^-10
10^-12
VT0
VT1
VT2
Vg2=-1.0 V
Vg2=-0.5 V
Vg2=Vg1
-1.0
-0.50
0.0
0.50
1.0
1.5
Gate 1 input voltage, Vg1 (V)

FIG. 4

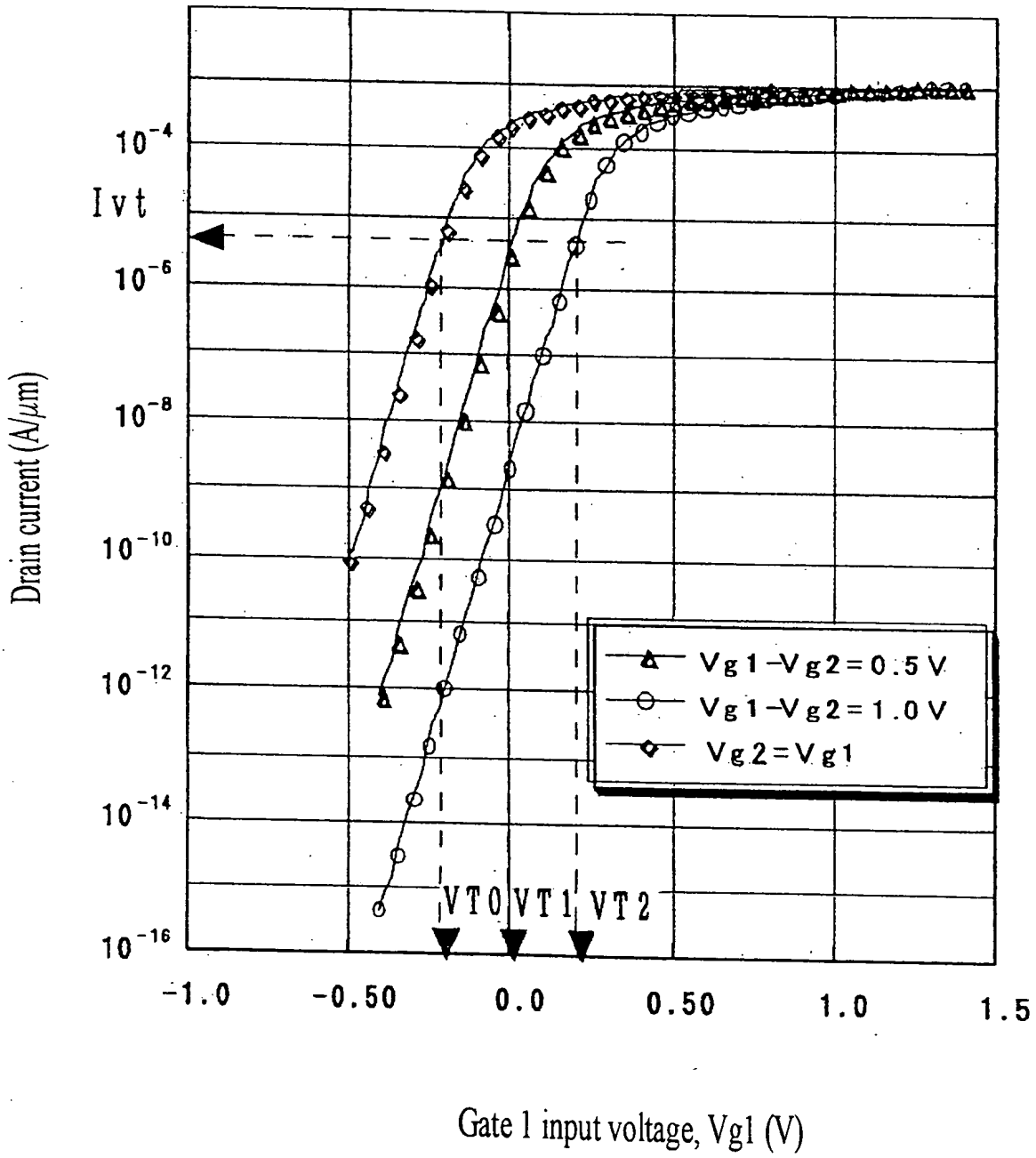

Drain current (A/μm)
10^-4
Ivt
10^-6
10^-8
10^-10
10^-12
10^-14
10^-16
VT0
VT1
VT2
Vg1-Vg2=0.5V
Vg1-Vg2=1.0V
Vg2=Vg1
-1.0
-0.50
0.0
0.50
1.0
1.5
Gate 1 input voltage, Vg1 (V)

FIG. 5

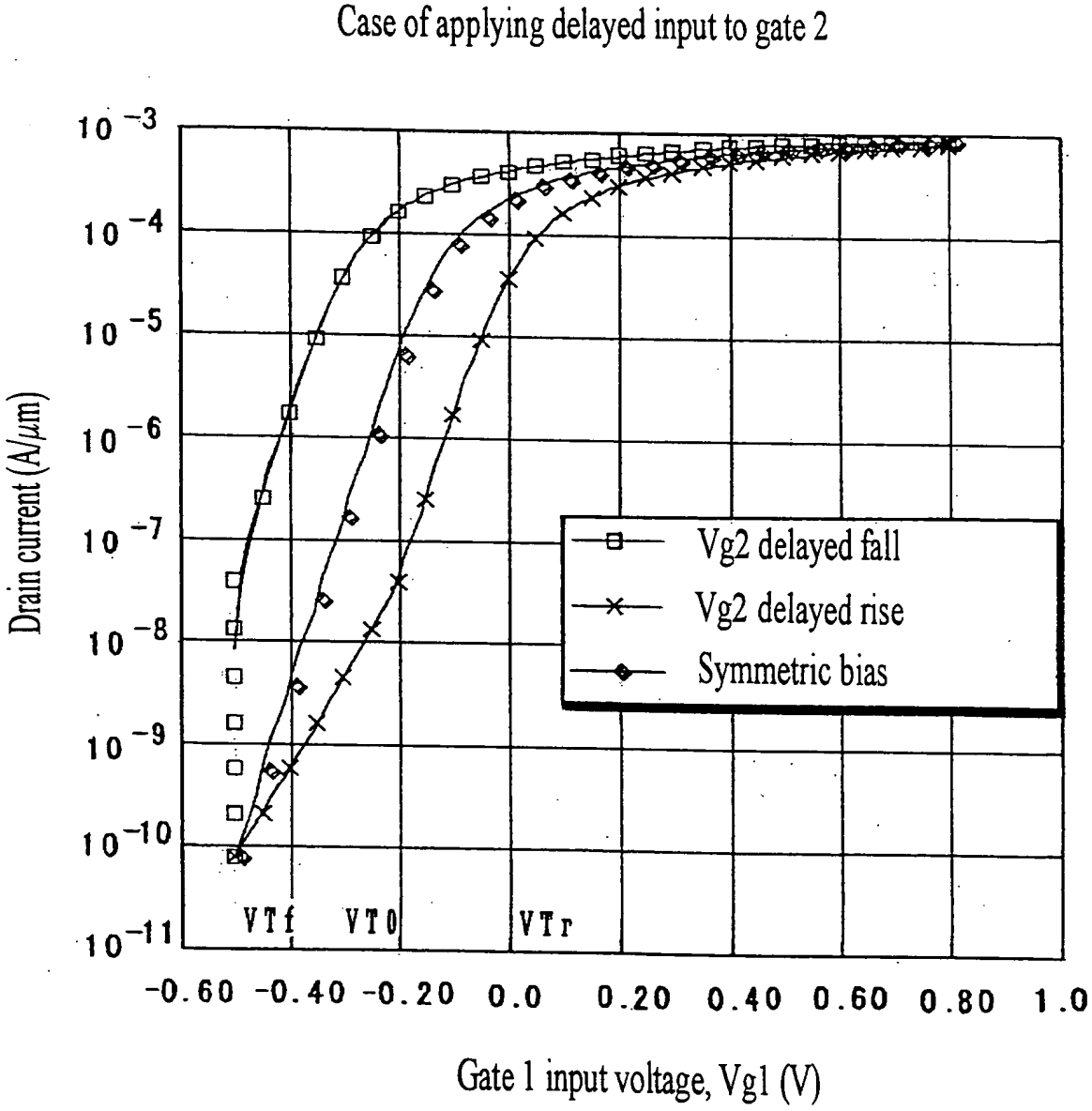

Case of applying delayed input to gate 2
Drain current (A/μm)
10 −3
10 −4
10 −5
10 −6
10 −7
10 −8
10 −9
10 −10
10 −11
VTf
VT0
VTr
Vg2 delayed fall
Vg2 delayed rise
Symmetric bias
-0.60 -0.40 -0.20 0.0 0.20 0.40 0.60 0.80 1.0
Gate 1 input voltage, Vg1 (V)

FIG. 6

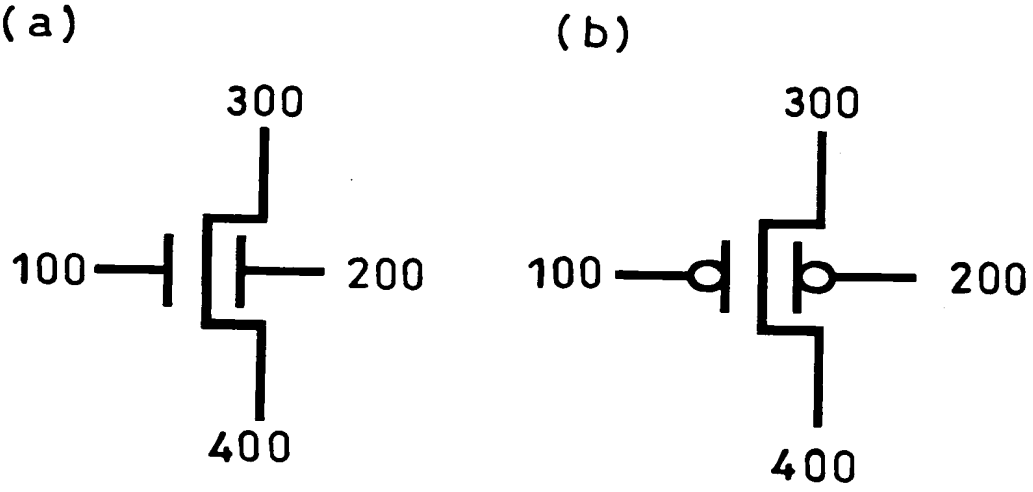

(a)
300
100
200
400
(b)
300
100
200
400

FIG. 7

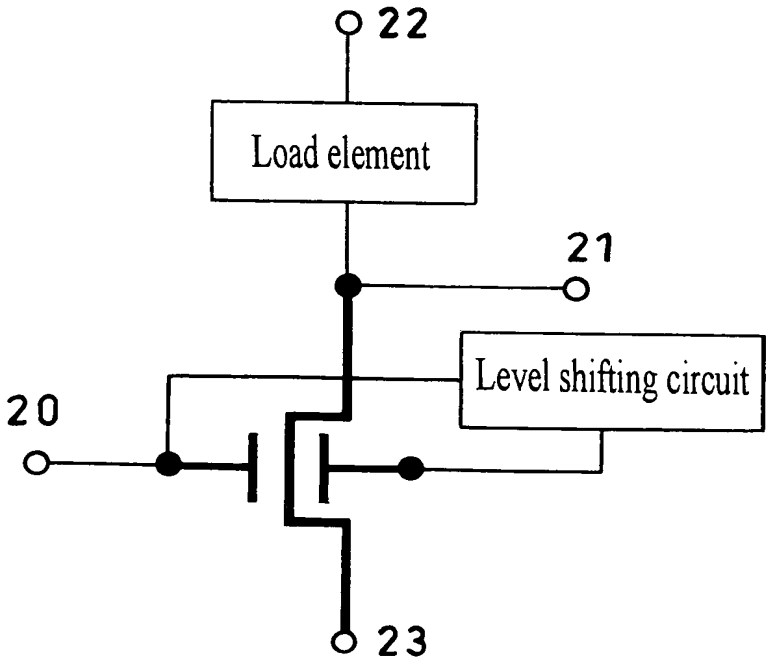

22
Load element
21
Level shifting circuit
20
23

FIG. 8

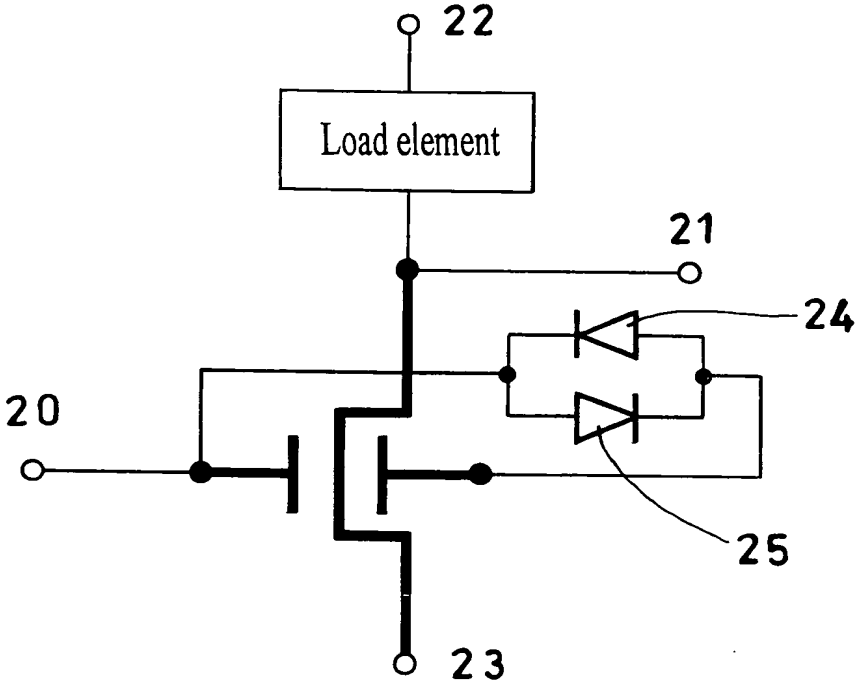

22
Load element
21
24
20
25
23

FIG. 9

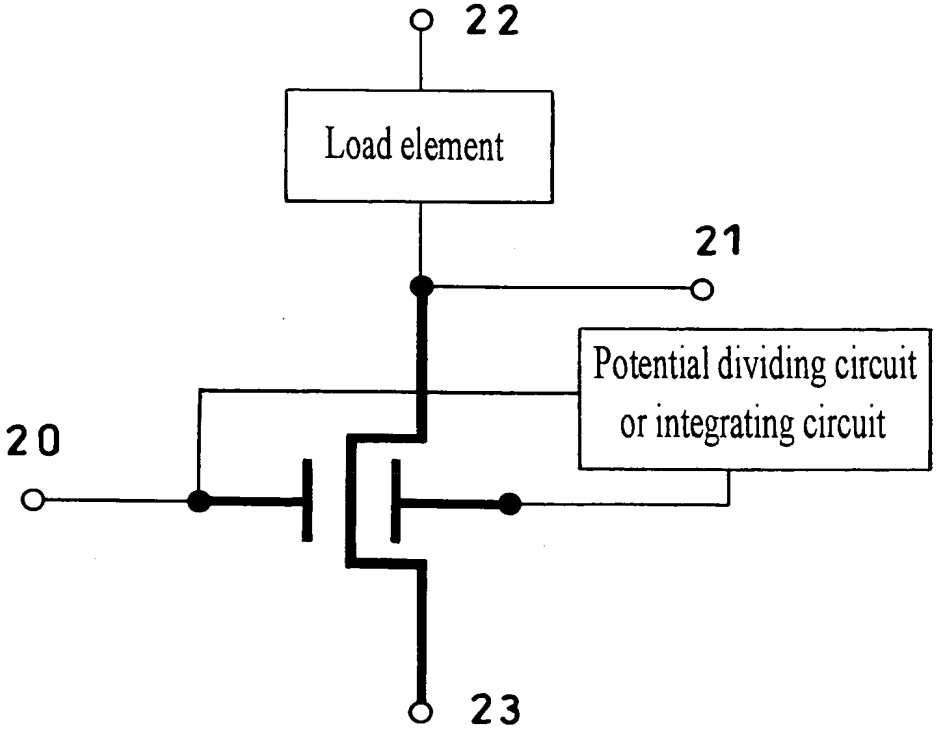

22
Load element
21
Potential dividing circuit
or integrating circuit
20
23

FIG. 10

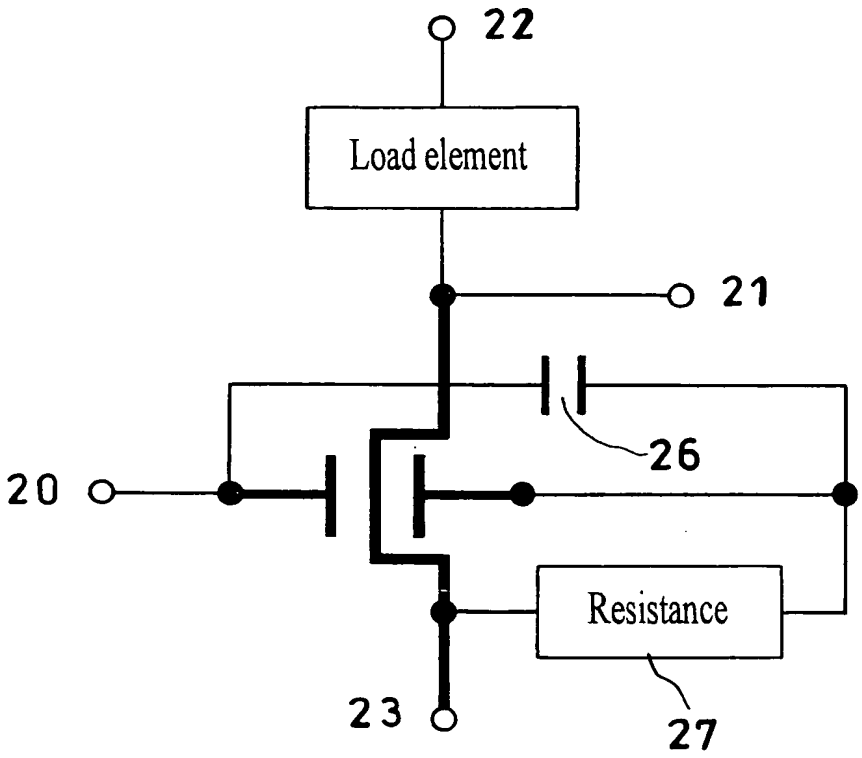
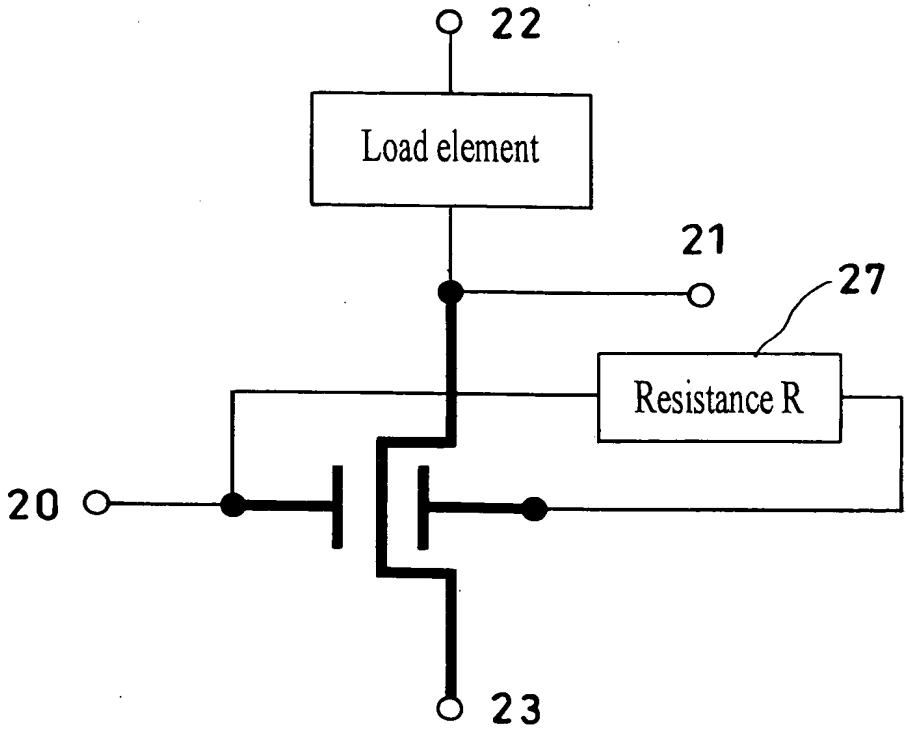

22
Load element
21
26
20
Resistance
23
27

FIG. 11


22
Load element
21
27
Resistance R
20
23

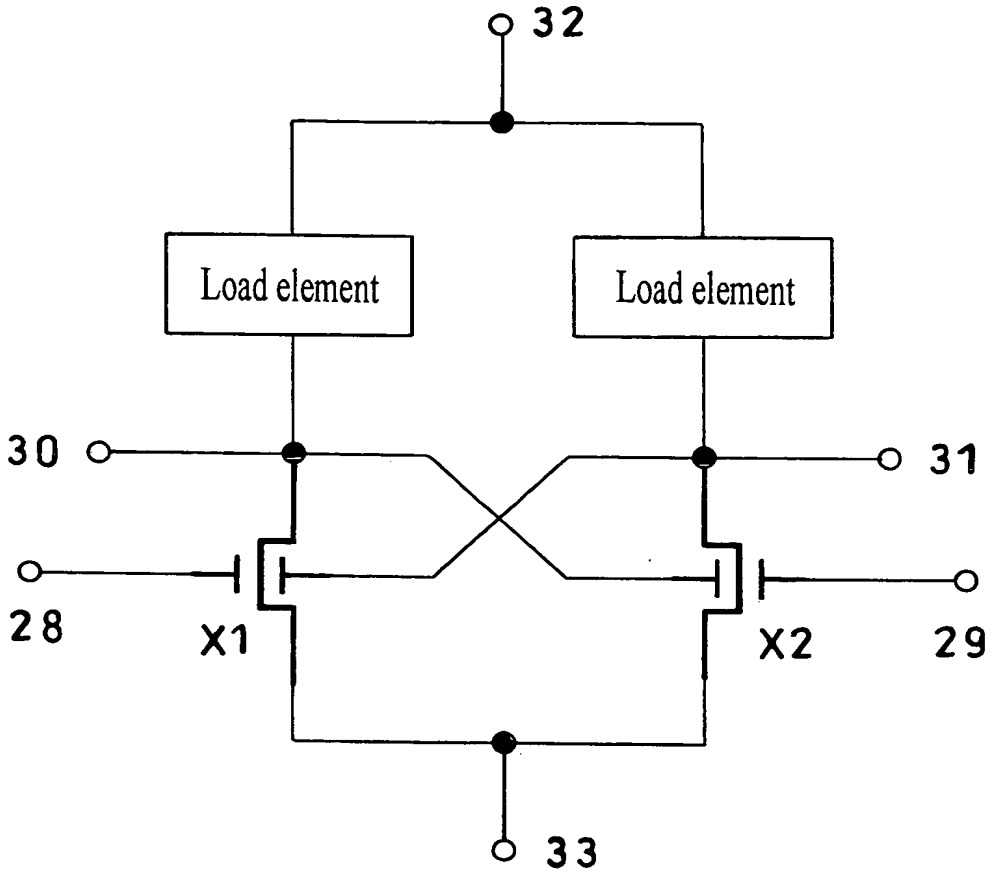



FIG. 12